AMENDMENTS TO THE SPECIFICATION

Please replace Paragraphs [0011], [0012], [0014], [0017] - [0020], [0023], [0025], [0027] - [0029] with the following paragraphs rewritten in amendment format:

[0011] FIG. 1 depicts a block diagram of a multi-service platform system 100 according to one embodiment of the invention. Multi-service platform system 100 can include a multi-service platform system chassis, with software and any number of slots for inserting nodes, for example, switch nodes 102, 104 and payload nodes 106, 108. Packet switched backplane 110 is used for connecting nodes placed in slots. As an example of an embodiment, a multi-service platform system 100 can include a chassis having model MVME5100 manufactured by Motorola Computer Group, 2900 South Diablo Way, Tempe, Ariz. 85282. The invention is not limited to this model or manufacturer and any multi-service platform system is included within the scope of the invention.

[0012] As shown in FIG. 1, multi-service platform system 100 can comprise a switch node 102, 104 coupled to any number of payload nodes 106, 108 via packet switched backplane 110. Payload ~~node~~nodes 106, 108 can add functionality to multi-service platform system 100 through the addition of processors, memory, storage devices, I/O elements, and the like. In other words, payload ~~node~~nodes 106, 108 can include any combination of processors, memory, storage devices, I/O elements, and the like, to give multi-service platform 100 the functionality desired by a user. In an embodiment, there are 18 payload slots for 18 payload nodes in multi-service platform system 100. However, any number of payload slots and payload nodes are included in the scope of the invention.

[0014] In one embodiment, packet switched backplane 110 can be an embedded packet switched backplane as is known in the art. In another embodiment, packet switched backplane 110 can be an overlay packet switched backplane that is overlaid on top of a backplane that does not have packet switched capability. In any embodiment of the invention, switch ~~node~~nodes 102, 104 is coupled to payload ~~node~~nodes 106, 108 via packet switched backplane 110. In an embodiment, packet switched backplane 110 comprises plurality of packet-based links 112 capable of ~~transmitted~~transmitting packet-based ~~signal~~signals 115 from/to switch ~~node~~nodes 102, 104 and payload ~~node~~nodes 106, 108. As an example of an embodiment, each of plurality of packet-based links 112 can comprise two 100-ohm differential signaling pairs.

[0017] In an embodiment, switch node 102 can receive any number of DS3 signals 114, 116. DS3 ~~signal~~signals 114, 116 each ~~represents~~represent a one of a series of standard digital transmission rates based on DS0, a transmission rate of 64 kilobites per second (Kbps), the bandwidth normally used for one telephone voice channel., DS3, the signal in a T-3 carrier, carries a multiple of 672 DS0 signals or 44.74 ~~Megabites~~Megabits per second (Mbps). In a particular embodiment, but not limiting of the invention, switch node 102 can include twelve DS3 signals 114, 116.

[0018] Switch node 102 can include, for each DS3 signal, DS3 signal interface unit 118, 120, which can be the physical connection allowing switch node 102 to receive DS3 ~~signal~~signals 114, 116. For example, DS3 interface unit can include a BNC or TNC type connector for DS3 signals as is known in the art. DS3 ~~signal~~signals 114, 116 can

enter switch node 102 on either the front panel or on a rear transition module of a chassis. Each DS3 signal 114, 116 is then interfaced to logic unit 122.

[0019] Logic unit 122 can comprise a serializer/de-serializer (serdes) 124 to de-serialize DS3 ~~signal~~signals 114, 116. Logic unit 122 can also comprise a buffer 126 to provide temporary storage for DS3 data from DS3 signals 114, 116. Logic unit 122 can further comprise crosspoint switch function 128 to allow mapping and remapping of DS3 signals to payload nodes 106, 108. Logic unit 122 translates DS3 ~~signal~~signals 114, 116 to packet-based ~~signal~~signals 115 so that data from DS3 ~~signal~~signals 114, 116 can be distributed to one or more of payload nodes 106, 108 as packet-based ~~signal~~signals 115 via packet switched backplane 110. In an embodiment, logic unit 122 can be a field programmable gate array (FPGA), and the like.

[0020] Software blocks that perform embodiments of the invention are part of computer program modules comprising computer instructions, such as control algorithms, that are stored in a computer-readable medium such as memory at logic unit 122. Computer instructions can instruct processors to perform methods of receiving and processing DS3 signals in a multi-service platform system 100, particularly at switch ~~node~~nodes 102, 104. In other embodiments, additional modules could be provided as needed.

[0023] Switch node 102 is coupled to any number of payload nodes 106, 108 via packet switched backplane 110 having a plurality of packet-based links 112. In an embodiment, multi-service platform system 100 can include a second switch node 104 coupled to payload nodes 106, 108. Second switch node 104 can have components

(not shown for clarity) analogous to switch node 102. Second switch node 104 can receive any number of DS3 signals 140, 142 analogous to switch node 102.

[0025] A second payload node 108 can be coupled to packet switched backplane 110 via packet-based interface 168. A packet-based interface 168 is included for each switch node that is coupled to payload node 108. In an example of an embodiment, each packet-based interface 168 can be a standard 100BaseT Ethernet physical connection. Gasketing logic 170 is coupled to packet-based interface 168 to provide a physical interface between the electrical standards of the packet-based interface 168 and receiver 172. In an embodiment, payload node 108 includes receiver 172, which can be a standard DS3 signal receiver such as a TEMUX, and the like. In another embodiment, receiver 172 can be designed for any custom implementation of processing data from DS3 signal. In an embodiment, payload node 108 can include more than one receiver 172, as each packet-based link 112 can carry more than one DS3 signal as discussed below. Receiver 172 is coupled to processor 174, which in an embodiment, can include a digital signal processor (DSP) and cluster support in order to process DS3 signal.

[0027] Since each of packet-based links can carry two DS3 signals, fault tolerance can be provided in multi-service platform system 100 for failure of a DS3 component on either switch ~~node~~nodes 102, 104 or payload ~~node~~nodes 106, 108. In one embodiment, fault tolerance is provided at the system level by including two packet-based interfaces 160 on each payload node 106 allowing simultaneous coupling to two

switch nodes 102, 104. In this case, 2X redundancy is provided in each payload node. However, it is possible to double the number of receivers 164 on each payload node 106 to provide an active+active configuration in which maximum functionality is available during normal operation with a halving of capacity should a switch node fail. In the case of failure, management software at the system level can reconfigure DS3 signal mapping (remapping) using logic unit 122, in particular crosspoint switch function 128, on switch node 102. In this embodiment, distribution of DS3 signals to one or more of plurality of payload nodes 106, 108 is transparent and details of the distribution are hidden above the hardware level with no impact at a software level.

[0028] FIG.2 illustrates a flow diagram 200 according to an embodiment of the invention. In step 202, DS3 signals are received at a switch node of a multi-service platform system 100. In step 204, DS3 signal is translated to a packet-based signal at the switch node. This can be accomplished in the logic unit of the switch node where the DS3 signal is de-serialized and put into packet format. In this way, the DS3 signal can be sent across packet switched backplane 110 to any number of payload nodes.

[0029] In step 206, data from DS3 signal, as the packet-based signal, is distributed to one or more of payload nodes via the packet switched backplane. DS3 signals are then received and processed at the one or more payload nodes. In step 208, in case of a fault, distribution of DS3 signals can be remapped to one or more payload nodes by a switch node, in particular logic unit 122 at the switch node.